MOSTEK®

4096 x 1-BIT DYNAMIC RAM

MK4027(J/N)-2/3

IV

FEATURES

- ☐ Industry standard 16-pin DIP (MK 4096) configuration
- ☐ 120ns access time, 320ns cycle (MK4027-1)
  150ns access time, 320ns cycle (MK4027-2)
  200ns access time, 375ns cycle (MK4027-3)
- ☐ ±10% tolerance on all supplies (+12V, ±5V)
- ☐ ECL compatible on V_{BB} power supply (–5.7V)
- ☐ Low Power: 462mW active (max)
  27mW standby (max)
- ☐ Improved performance with "gated $\overline{CAS}$", "$\overline{RAS}$ only" refresh and page mode capability
- ☐ All inputs are low capacitance and TTL compatible
- ☐ Input latches for addresses, chip select and data in
- ☐ Three-state TTL compatible output
- ☐ Output data latched and valid into next cycle
- ☐ MKB version screened to MIL-STD-883

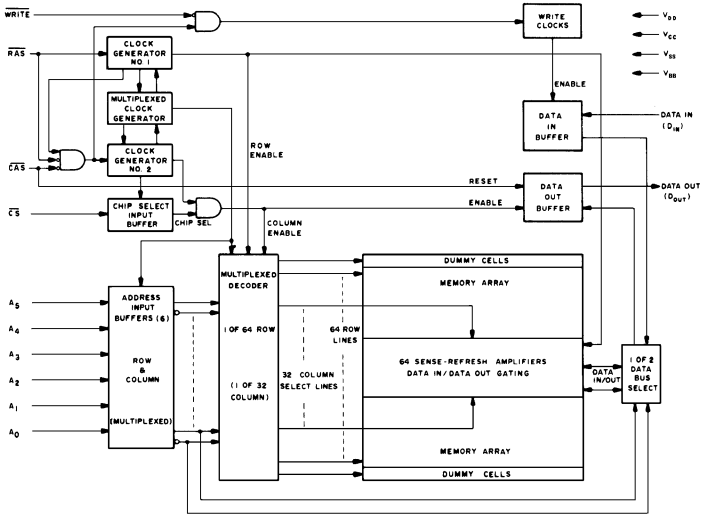
DESCRIPTION

The MK 4027 is a 4096 word by 1 bit MOS random access memory circuit fabricated with MOSTEK's N-channel silicon gate process. This process allows the MK 4027 to be a high performance state-of-the-art memory circuit that is manufacturable in high volume. The MK 4027 employs a single transistor storage cell utilizing a dynamic storage technique and dynamic control circuitry to achieve optimum performance with low power dissipation.

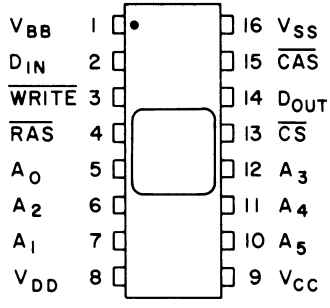
A unique multiplexing and latching technique for the address inputs permits the MK 4027 to be packaged in a standard 16-pin DIP on 0.3 in. centers. This package size provides high system-bit densities and is compatible with widely available automated testing and insertion equipment.

System oriented features include direct interfacing capability with TTL, only 6 very low capacitance address lines to drive, on-chip address and data registers which eliminates the need for interface registers, input logic levels selected to optimize noise immunity, and two chip select methods to allow the user to determine the appropriate speed/power characteristics of his memory system. The MK 4027 also incorporates several flexible operating modes. In addition to the usual read and write cycles, read-modify write, page-mode, and $\overline{RAS}$-only refresh cycles are available with the MK 4027. Page-mode timing is very useful in systems requiring Direct Memory Access (DMA) operation.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



PIN NAMES

A_0-A_5	ADDRESS INPUTS
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{CS}$	CHIP SELECT
D_{IN}	DATA IN
D_{OUT}	DATA OUT
$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{WRITE}$	READ/WRITE INPUT
V_{BB}	POWER (–5V)
V_{CC}	POWER (+5V)
V_{DD}	POWER (+ 12V)
V_{SS}	GROUND

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{BB} ..... −0.5V to +20V
Voltage on V_{DD}, V_{CC} relative to V_{SS} ..... −1.0V to +15V
$V_{BB}-V_{SS}$ ($V_{DD}-V_{SS} > 0$) 0V
Operating temperature, T_A (Ambient) ..... 0°C to + 70°C
Storage temperature (Ambient)(Ceramic) ..... −65°C to + 150°C
Storage temperature (Ambient)(Plastic) ..... −55°C to + 125°C
Short circuit output current 50mA
Power dissipation ..... 1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS [4]

($0°C \leqslant T_A \leqslant 70°C$) [1]

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{DD}	Supply Voltage	10.8	12.0	13.2	volts	2
V_{CC}	Supply Voltage	4.5V	5.0	5.5	volts	2,3
V_{SS}	Supply Voltage	0	0	0	volts	2
V_{BB}	Supply Voltage	−4.5	−5.0	−5.7	volts	2
V_{IHC}	Logic 1 Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.4		7.0	volts	2
V_{IH}	Logic 1 Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.2		7.0	volts	2
V_{IL}	Logic 0 Voltage, all inputs	−1.0		.8	volts	2

DC ELECTRICAL CHARACTERISTICS [4]

($0°C \leqslant T_A \leqslant 70°C$)[1] ($V_{DD}$ = 12.0V ± 10%; V_{CC} = 5.0V ± 10%; V_{SS} = 0V; $-5.7V \leqslant V_{BB} \leqslant -4.5V$)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
I_{DD1}	Average V_{DD} Power Supply Current			35	mA	5
I_{DD2}	Standby V_{DD} Power Supply Current			2	mA	8
I_{DD3}	Average V_{DD} Power Supply Current during "$\overline{RAS}$ only" cycles			25	mA	
I_{CC}	V_{CC} Power Supply Current				mA	6
I_{BB}	Average V_{BB} Power Supply Current			150	μA	
$I_{I(L)}$	Input Leakage Current (any input)			10	μA	7
$I_{O(L)}$	Output Leakage Current			10	μA	8,9
V_{OH}	Output Logic 1 Voltage @ I_{OUT} = −5mA	2.4			volts	
V_{OL}	Output Logic 0 Voltage @ I_{OUT} = 3.2mA			0.4	volts	

NOTES

1. T_A is specified for operation at frequencies to $t_{RC} \geqslant t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible provided that all AC parameters are met. See figure 2 for derating curve.
2. All voltages referenced to V_{SS}.
3. Output voltage will swing from V_{SS} to V_{CC} when enabled,with no output load. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.
4. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
5. Current is proportional to cycle rate. I_{DD1} (max) is measured at the cycle rate specified by t_{RC} (min). See figure 1 for I_{DD1} limits at other cycle rates.
6. I_{CC} depends on output loading. During readout of high level data V_{CC} is connected through a low impedance (135Ω typ) to Data Out. At all other times I_{CC} consists of leakage currents only.
7. All device pins at 0 volts except V_{BB} which is at −5 volts and the pin under test which is at +10 volts.
8. Output is disabled (high impedance) and $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1. Transient stabilization is required prior to measurement of this parameter.
9. $0V \leqslant V_{OUT} \leqslant +10V$.
10. Effective capacitance is calculated from the equation:

$$C = \frac{\Delta Q}{\Delta V} \text{ with } \Delta V = 3 \text{ volts.}$$

11. A.C. measurements assume t_T = 5ns.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS(4, 11, 17)

($0°C \leq T_A \leq 70°C$)1 (V_{DD} = 12.0V ± 10%, V_{CC} = 5.0V ± 10%, V_{SS} = 0V, $-5.7V \leq V_{BB} \leq -4.5V$)

	PARAMETER	MK4027-2		MK4027-3		UNITS	NOTES
		MIN	MAX	MIN	MAX		
t_{RC}	Random read or write cycle time	320		375		ns	12
t_{RWC}	Read write cycle time	320		375		ns	12
t_{RMW}	Read modify write cycle time	320		405		ns	12
t_{PC}	Page mode cycle time	170		225		ns	12
t_{RAC}	Access time from row address strobe		150		200	ns	13, 15
t_{CAC}	Access time from column address strobe		100		135	ns	14, 15
t_{OFF}	Output buffer turn-off delay		40		50	ns	
t_{RP}	Row address strobe precharge time	100		120		ns	
t_{RAS}	Row address strobe pulse width	150	10,000	200	10,000	ns	
t_{RSH}	Row address strobe hold time	100		135		ns	
t_{CAS}	Column address strobe pulse width	100		135		ns	
t_{CSH}	Column address strobe hold time	150		200		ns	
t_{RCD}	Row to column strobe delay	20	50	25	65	ns	16
t_{ASR}	Row address set-up time	0		0		ns	
t_{RAH}	Row address hold time	20		25		ns	
t_{ASC}	Column address set-up time	−10		−10		ns	
t_{CAH}	Column address hold time	45		55		ns	
t_{AR}	Column address hold time referenced to $\overline{RAS}$	95		120		ns	
t_{CSC}	Chip select set-up time	−10		−10		ns	
t_{CH}	Chip select hold time	45		55		ns	
t_{CHR}	Chip select hold time referenced to $\overline{RAS}$	95		120		ns	
t_T	Transition time (rise and fall)	3	35	3	50	ns	17
t_{RCS}	Read command set-up time	0		0		ns	
t_{RCH}	Read command hold time	0		0		ns	
t_{WCH}	Write command hold time	45		55		ns	
t_{WCR}	Write command hold time referenced to $\overline{RAS}$	95		120		ns	
t_{WP}	Write command pulse width	45		55		ns	
t_{RWL}	Write command to row strobe lead time	50		70		ns	
t_{CWL}	Write command to column strobe lead time	50		70		ns	
t_{DS}	Data in set-up time	0		0		ns	18
t_{DH}	Data in hold time	45		55		ns	18
t_{DHR}	Data in hold time referenced to $\overline{RAS}$	95		120		ns	
t_{CRP}	Column to row strobe precharge time	0		0		ns	
t_{CP}	Column precharge time	60		80		ns	
t_{RFSH}	Refresh period		2		2	ms	
t_{WCS}	Write command set-up time	0		0		ns	19
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ delay	60		80		ns	19
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ delay	110		145		ns	19
t_{DOH}	Data out hold time	10		10		μs	

Notes Continued

12. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured. See figure 2 for derating curve.

13. Assumes that $t_{RCD} \leq t_{RCD}$ (max).

14. Assumes that $t_{RCD} \geq t_{RCD}$ (max).

15. Measured with a load circuit equivalent to 2 TTL loads and 100pF

16. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

17. V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.

18. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.

19. t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in a read/write or read/modify/write cycle only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and Data Out will contain the data written into the selected cell. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and Data Out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of Data Out (at access time) is indeterminate.

AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$) ($V_{DD} = 12.0V \pm 10\%$; $V_{SS} = 0V$; $-5.7V \leq V_{BB} \leq -4.5V$)

	PARAMETER	TYP	MAX	UNITS	NOTES
C_{I1}	Input Capacitance (A_0-A_5), D_{IN}, $\overline{CS}$	4	5	pF	10
C_{I2}	Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	8	10	pF	10
C_O	Output Capacitance (D_{OUT})	5	7	pF	8,10

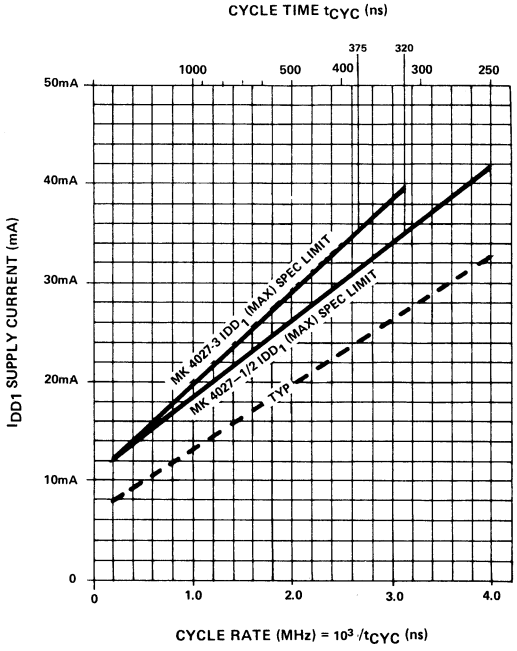


Figure 1. Maximum I_{DD1} versus cycle rate for device operation at extended frequencies.

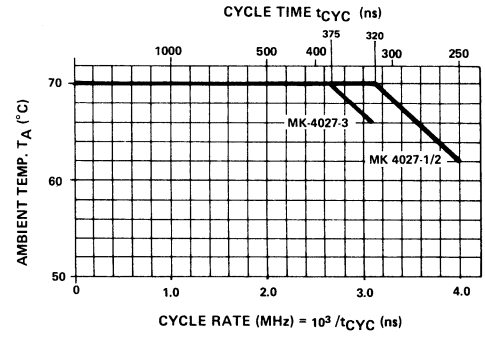
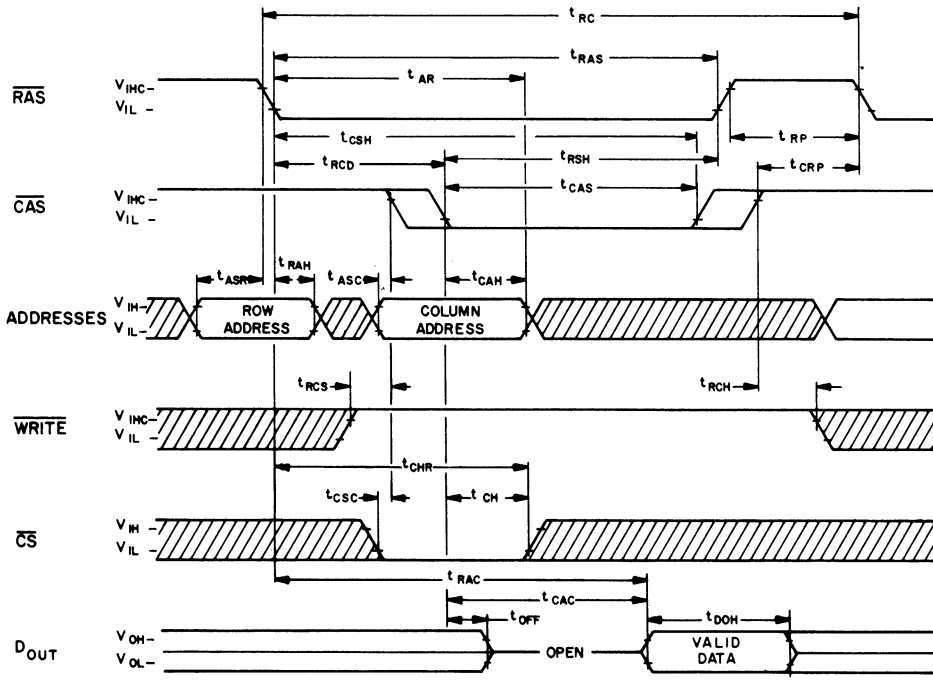
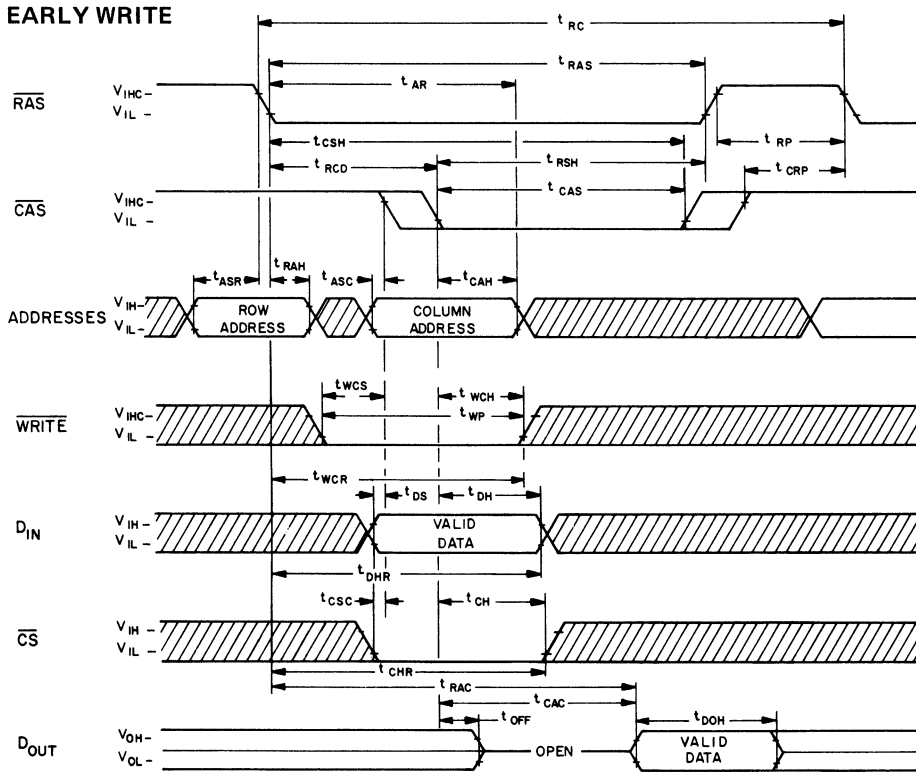


Figure 2. Maximum ambient temperature versus cycle rate for extended frequency operation.

READ CYCLE

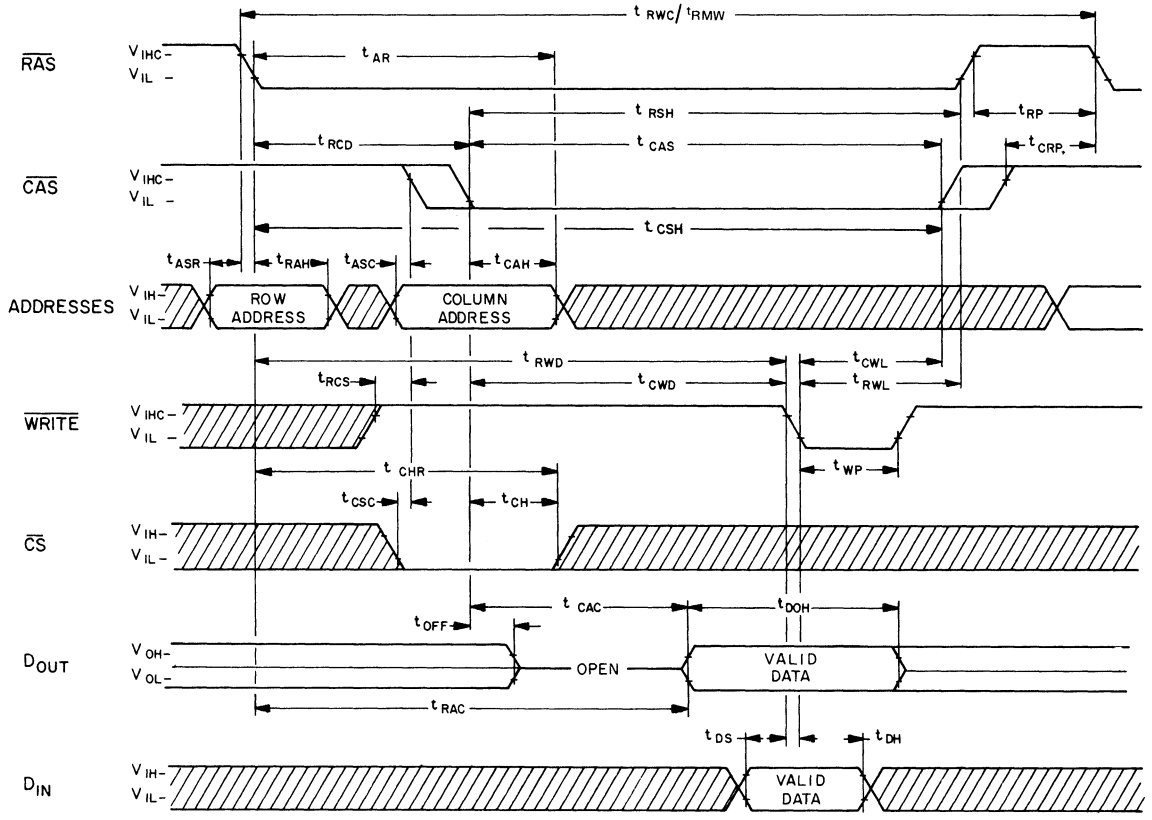


EARLY WRITE

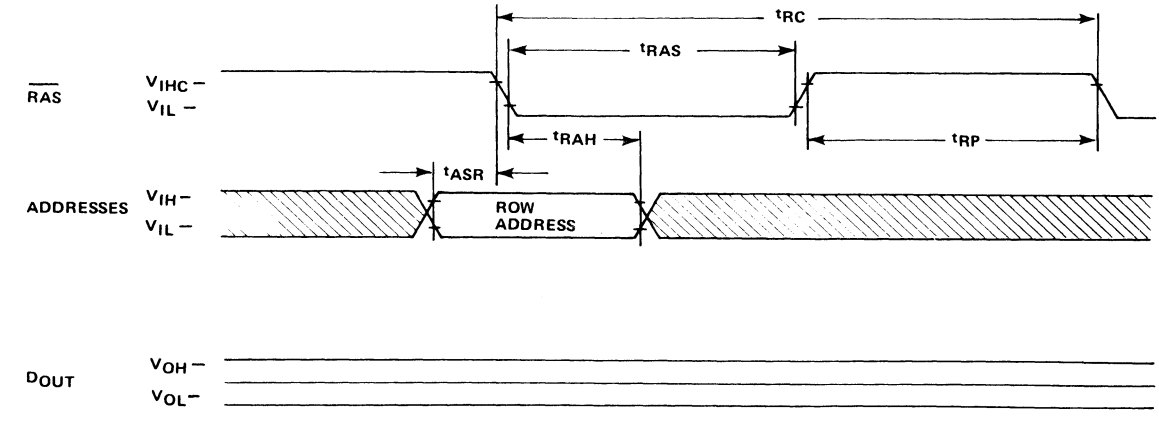


IV

READ-WRITE / READ-MODIFY-WRITE CYCLE

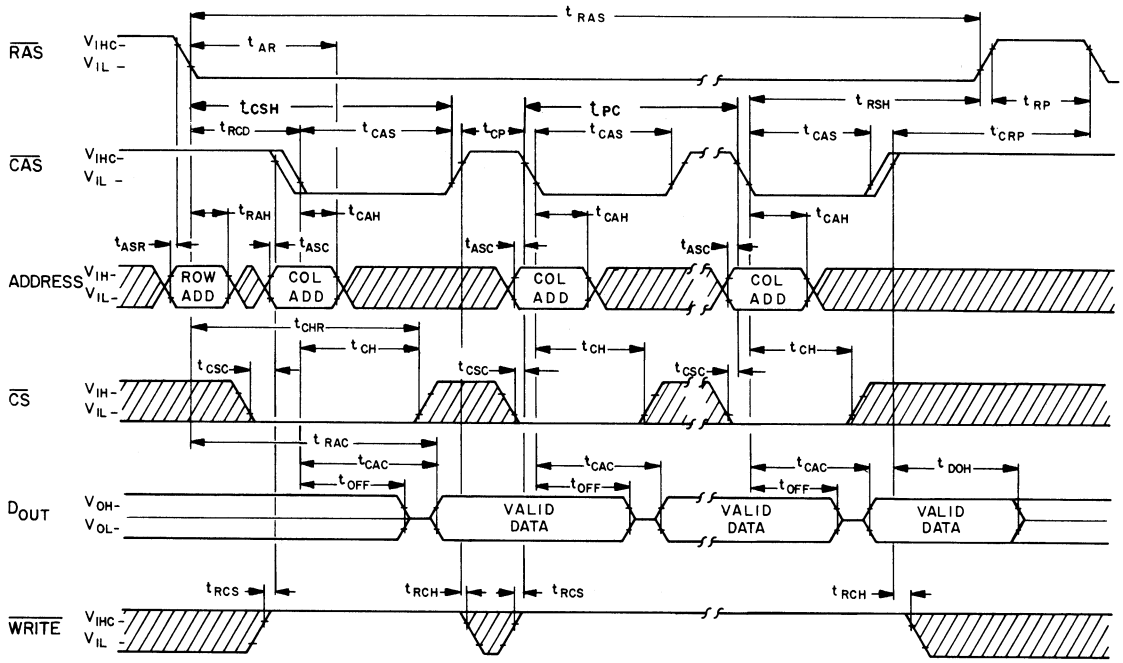


"RAS ONLY" REFRESH CYCLE

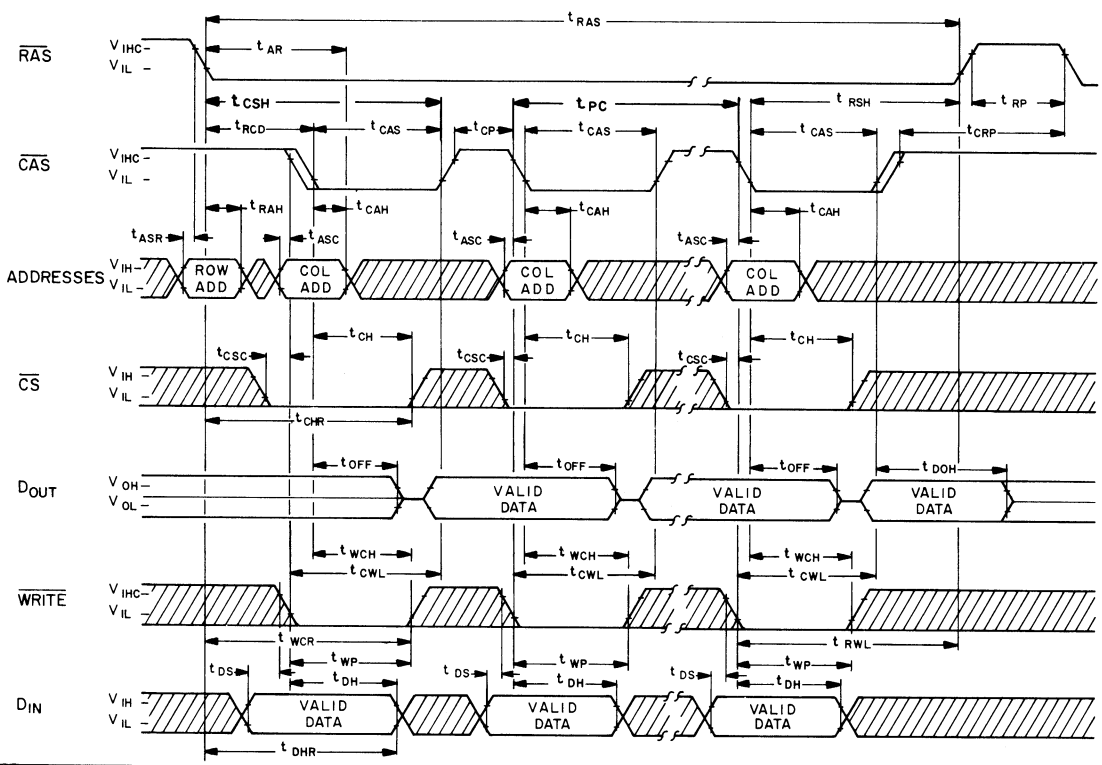


NOTE: D_{OUT} remains unchanged from previous cycle.

PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



ADDRESSING

The 12 address bits required to decode 1 of the 4096 cell locations within the MK 4027 are multiplexed onto the 6 address inputs and latched into the on-chip address latches by externally applying two negative going TTL level clocks. The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 6 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 6 column address bits plus Chip Select ($\overline{CS}$) into the chip. The internal circuitry of the MK 4027 is designed to allow the column information to be externally applied to the chip before it is actually required. Because of this, the hold time requirements for the input signals associated with the Column Address Strobe are also referenced to $\overline{RAS}$. However, this gated $\overline{CAS}$ feature allows the system designer to compensate for timing skews that may be encountered in the multiplexing operation. Since the Chip Select signal is not required until $\overline{CAS}$ time, which is well into the memory cycle, its decoding time does not add to system access or cycle time.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The later of the signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low prior to $\overline{CAS}$, the Data In is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. If the data input is not available at $\overline{CAS}$ time or if it is desired that the cycle be a read-write cycle, the $\overline{WRITE}$ signal must be delayed until after $\overline{CAS}$. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than to $\overline{CAS}$. (To illustrate this feature, Data In is referenced to $\overline{WRITE}$ in the timing diagram depicting the read-write and page mode write cycles while the "early write" cycle diagram shows Data In referenced to $\overline{CAS}$.) Note that if the chip is unselected ($\overline{CS}$ high at $\overline{CAS}$ time) $\overline{WRITE}$ commands are not executed and, consequently, data stored in the memory is unaffected.

Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{CAS}$ is active. Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT LATCH

Any change in the condition of the Data Out Latch is initiated by the $\overline{CAS}$ signal. The output buffer is not affected by memory (refresh) cycles in which only the $\overline{RAS}$ signal is applied to the MK 4027. Whenever $\overline{CAS}$ makes a negative transition, the output will go unconditionally open-circuited, independent of the state of any other input to the chip. If the cycle in progress is a read, read-modify-write, or a delayed write cycle and the chip is selected, then the output latch and buffer will again go active and at access time will contain the data read from the selected cell. This output data is the same polarity (not inverted) as the input data. If the cycle in progress is a write cycle ($\overline{WRITE}$ active low before $\overline{CAS}$ goes low) and the chip is selected, then at access time the output latch and buffer will contain the input data. Once having gone active, the output will remain valid until the MK 4027 receives the next $\overline{CAS}$ negative edge. Intervening refresh cycles in which a $\overline{RAS}$ is received (but no $\overline{CAS}$) will not cause valid data to be affected. Conversely, the output will assume the open-circuit state during any cycle in which the MK 4027 receives a $\overline{CAS}$ but no $\overline{RAS}$ signal (regardless of the state of any other inputs). The output will also assume the open circuit state in normal cycles (in which both $\overline{RAS}$ and $\overline{CAS}$ signals occur) if the chip is unselected.

The three-state data output buffer presents the data output pin with a low impedance to V_{CC} for a logic 1 and a low impedance to V_{SS} for a logic 0. The output resistance to V_{CC} (logic 1 state) is 420 Ω maximum and 135 Ω typically. The output resistance to V_{SS} (logic 0 state) is 125 Ω maximum and 35 Ω typically. The separate V_{CC} pin allows the output buffer to be powered from the supply voltage of the logic to which the chip is interfaced. During battery standby operation, the V_{CC} pin may have power removed without affecting the MK 4027 refresh operation. This allows all system logic except the $\overline{RAS}$ timing circuitry and the refresh address logic to be turned off during battery standby to conserve power.

REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 64 row addresses within each 2 millisecond time interval. Any cycle in which a $\overline{RAS}$ signal occurs, accomplishes a refresh operation. A read cycle will refresh the selected row, regardless of the state of the Chip Select ($\overline{CS}$) input. A write or read-modify-write cycle also refreshes the selected row, but the chip should be unselected to prevent writing data into the selected cell. If, during a refresh cycle, the MK 4027 receives a $\overline{RAS}$ signal but no $\overline{CAS}$ signal, the state of the output will not be affected. However, if "$\overline{RAS}$-only" refresh cycles (where $\overline{RAS}$ is the only signal applied to the chip) are continued for extended periods, the output buffer may eventually lose proper data and go open-circuit. The output buffer will regain activity with the first cycle in which a $\overline{CAS}$ signal is applied to the chip.

POWER DISSIPATION/STANDBY MODE

Most of the circuitry used in the MK 4027 is dynamic and most of the power drawn is the result of an address strobe edge. Because the power is not drawn during the whole time the strobe is active, the dynamic power is a function of operating frequency rather than active duty cycle. Typically, the power is 170mW at 1 μsec cycle rate for the MK 4027 with a worse case power of less than 470mW at 320nsec cycle time. To minimize the overall system power, the Row Address Strobe ($\overline{RAS}$) should be decoded and supplied to only the selected chips. The $\overline{CAS}$ must be supplied to all chips (to turn off the unselected output). Those chips that did not receive a $\overline{RAS}$, however, will not dissipate any power on the $\overline{CAS}$ edges, except for that required to turn off the outputs. If the $\overline{RAS}$ signal is decoded and supplied only to the selected chips, then the Chip Select ($\overline{CS}$) input of all chips can be at a logic 0. The chips that receive a $\overline{CAS}$ but no $\overline{RAS}$ will be unselected (output open-circuited) regardless of the Chip Select input. For refresh cycles, however, either the $\overline{CS}$ input of all chips must be high or the $\overline{CAS}$ input must be held high to prevent several "wire-OR'd" outputs from turning on with opposing force. Note that the MK 4027 will dissipate considerably less power when the refresh operation is accomplished with a "$\overline{RAS}$-only" cycle as opposed to a normal $\overline{RAS}/\overline{CAS}$ memory cycle.

PAGE MODE OPERATION

The "Page Mode" feature of the MK 4027 allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and keeping the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "page mode" of operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$. Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times. The chip select input ($\overline{CS}$) is operative in page mode cycles just as in normal cycles. It is not necessary that the chip be selected during the first operation in a sequence of page cycles. Likewise, the $\overline{CS}$ input can be used to select or disable any cycle(s) in a series of page cycles. This feature allows the page boundary to be extended beyond the 64 column locations in a single chip. The page boundary can be extended by applying $\overline{RAS}$ to multiple 4K memory blocks and decoding $\overline{CS}$ to select the proper block.

POWER UP

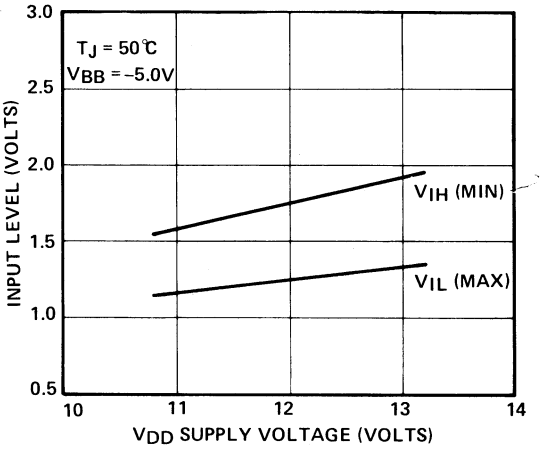
The MK 4027 requires no particular power supply sequencing so long as the Absolute Maximum Rating Conditions are observed. However, in order to insure compliance with the Absolute Maximum Ratings, MOSTEK recommends sequencing of power supplies such that V_{BB} is applied first and removed last. V_{BB} should never be more positive than V_{SS} when power is applied to V_{DD}.

Under system failure conditions in which one or more supplies exceed the specified limits significant additional margin against catastrophic device failure may be achieved by forcing $\overline{RAS}$ and Data Out to the inactive state.

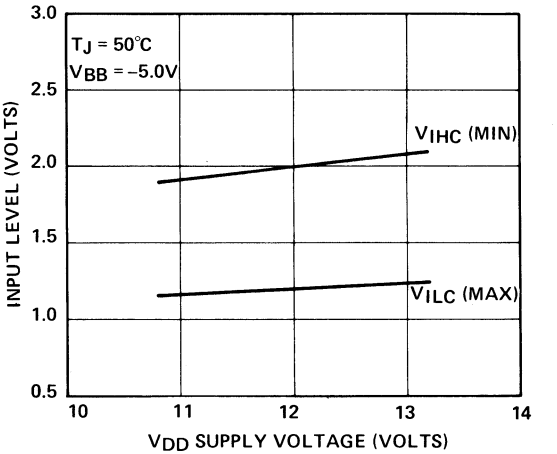
After power is applied to the device, the MK 4027 requires several cycles before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.

TYPICAL DEVICE CHARACTERISTICS

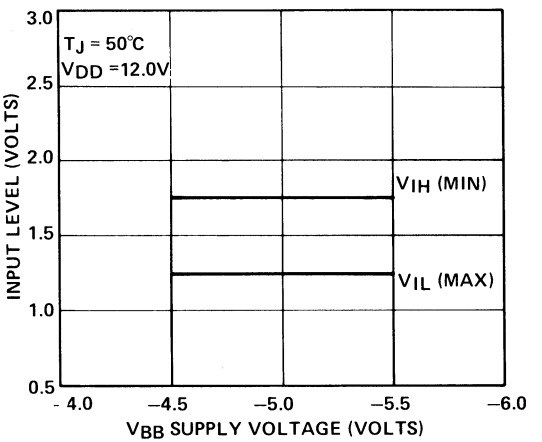
TYPICAL ADDRESS AND DATA INPUT LEVELS vs. V_{DD}



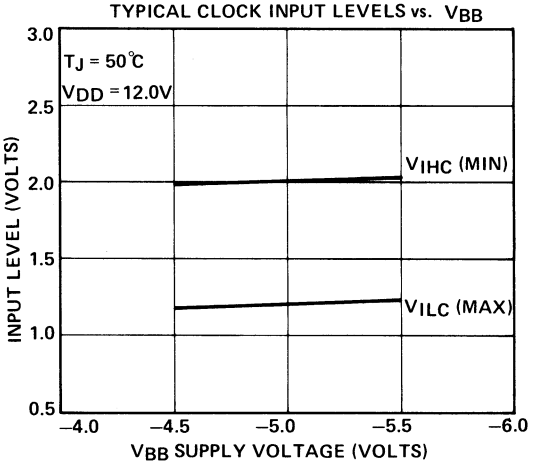
TYPICAL CLOCK INPUT LEVELS vs. V_{DD}



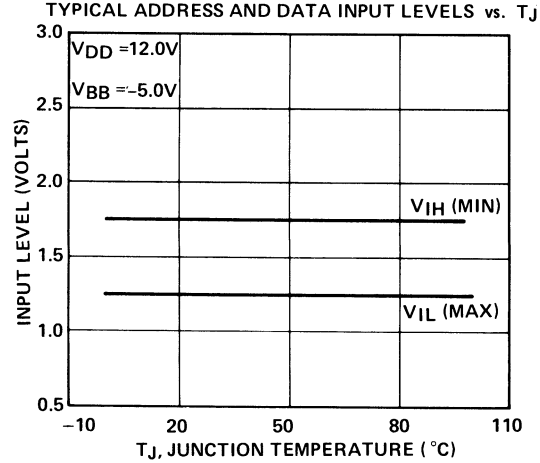
TYPICAL ADDRESS AND DATA INPUT LEVELS vs. V_{BB}



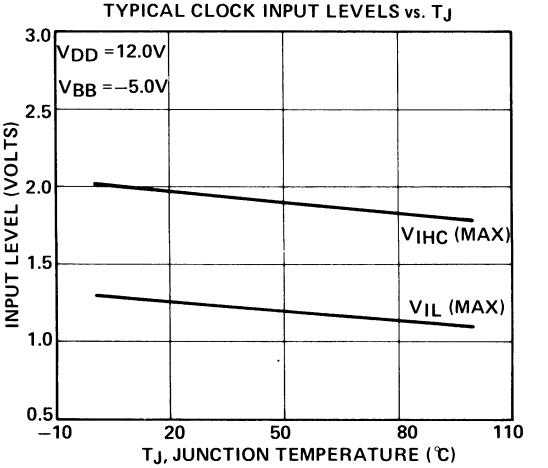
TYPICAL CLOCK INPUT LEVELS vs. V_{BB}



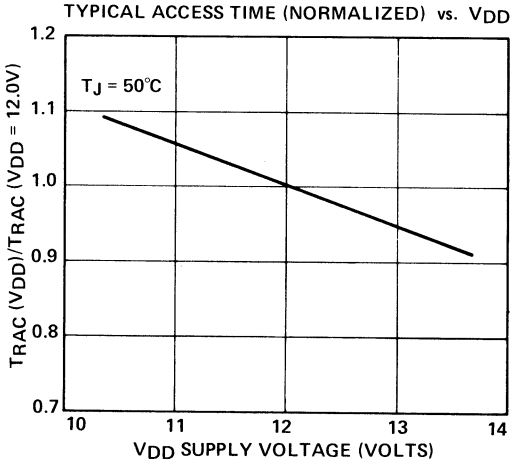
TYPICAL ADDRESS AND DATA INPUT LEVELS vs. T_J



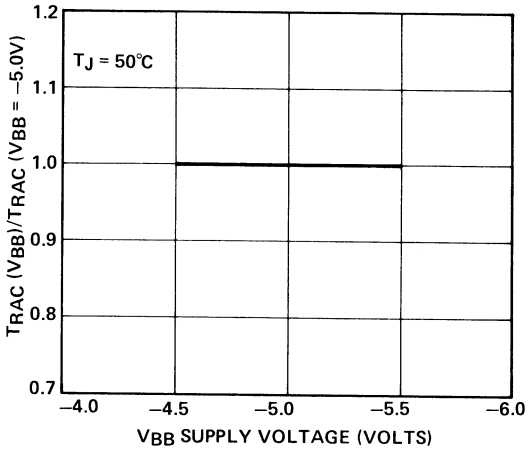
TYPICAL CLOCK INPUT LEVELS vs. T_J



TYPICAL ACCESS TIME (NORMALIZED) vs. V_{DD}

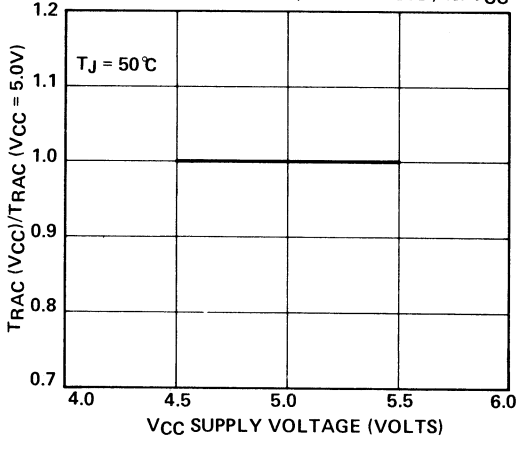


TYPICAL ACCESS TIME (NORMALIZED) vs. V_{BB}

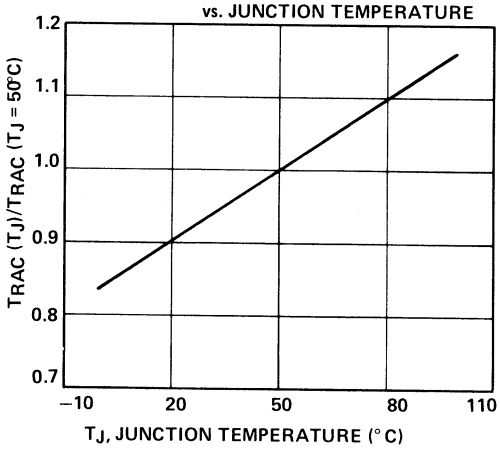


IV

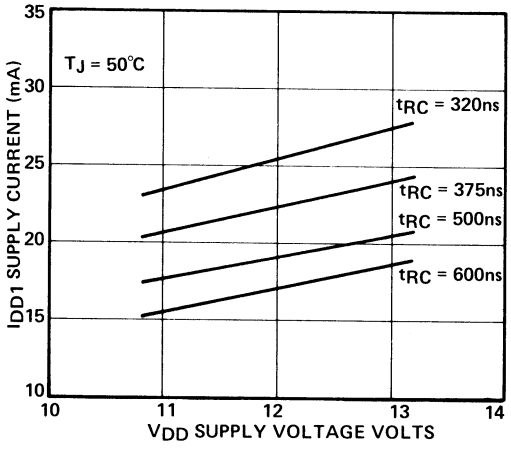
TYPICAL ACCESS TIME (NORMALIZED) vs. V_{CC}



TYPICAL ACCESS TIME (NORMALIZED) vs. JUNCTION TEMPERATURE



TYPICAL I_{DD1} vs. V_{DD}



TYPICAL I_{DD1} vs. JUNCTION TEMPERATURE